CLAIMS

What is claimed is:

1. A serial peripheral interface device configured for providing a high performance buffering scheme for transmitting data to and receiving data from another peripheral device, said serial peripheral interface device comprising:

an input/output control device for interfacing with the other peripheral device; and

a single buffer having a transmit shift register, a receive shift register, a data register and a queuing arrangement, wherein said queuing arrangement comprises a pointer/counter arrangement and is configured to provide for the receiving of new data in said data register at substantially the same time as stored data is transmitted from said register.

2. A serial peripheral interface device according to claim 1, wherein said queuing arrangement comprises a circular queuing arrangement.

3. A serial peripheral interface device according to claim 1, wherein said queuing arrangement comprises a linear queuing arrangement.

4. A serial peripheral interface device according to claim 1, wherein said queuing arrangement comprises:

a write pointer configured to indicate a location in said single buffer where a CPU can write data to be transmitted;

a read pointer configured to identify a location in said single buffer where any received data can be stored for reading by the CPU; and

a shift pointer configured to identify a location for data to be transmitted and a location where the received data will be stored after shifting of any registers is completed.

5. A serial peripheral interface device according to claim 4, wherein said queuing arrangement further comprises:

a write counter configured to numerically track any bytes of data that need to be transmitted; and

a read counter configured to numerically track any bytes of data that have been received.

6. A serial peripheral interface device according to claim 1, wherein said queuing arrangement further comprises

a circular FIFO buffer configured for at least 32 bytes.

7. A serial peripheral interface device according to claim 5, wherein said serial peripheral interface device comprises two interrupt requests configured to facilitate a reduction in polling by a CPU.

8. A serial peripheral interface device according to claim 7, wherein said two interrupt requests comprise a transmit interrupt request configured with a first threshold value and a receive interrupt request configured with a second threshold value.

9. A microcontroller-based data communication device configured with a serial peripheral interface device to provide a high performance buffering scheme for transmitting and receiving data, said serial peripheral interface device comprising:

an input/output control device for interfacing with peripheral devices; and

a single buffer having a transmit shift register, a receive shift register, a data register and a queuing arrangement, wherein said queuing arrangement comprises a pointer/counter arrangement and is configured to provide for the receiving of new data in said data register at substantially the same time as stored data is transmitted from said data register.

10. A serial peripheral interface device according to claim 1, wherein said queuing arrangement comprises at least one of a circular queuing arrangement and a linear queuing arrangement.

11. A serial peripheral interface device according to claim 9, wherein said queuing arrangement comprises:

a write pointer configured to indicate a location in said single buffer where a CPU can write data to be transmitted;

a read pointer configured to identify a location in said single buffer where any received data can be stored for reading by the CPU; and

a shift pointer configured to identify a location for data to be transmitted and a location where the received data will be stored after shifting of any registers is completed.

12. A serial peripheral interface device according to claim 11, wherein said queuing arrangement further comprises:

a write counter configured to numerically track any bytes of data that need to be transmitted; and

a read counter configured to numerically track any bytes of data that have been received.

13. A serial peripheral interface device according to claim 12, wherein said serial peripheral interface device comprises two interrupt requests configured to facilitate a reduction in polling by a CPU.

14. A serial peripheral interface device according to claim 13, wherein said two interrupt requests comprise a transmit interrupt request configured with a first threshold value and a receive interrupt request configured with a second threshold value.

15. A high performance buffering technique for use with a serial peripheral interface to facilitate high data rates, said buffering technique comprising the steps of:

initializing a buffer by writing data to a data register;

performing a transmit buffering sequence to prepare for the transmitting of the data;

performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time; and

performing a receive buffering sequence to prepare for the receipt of additional new data.

16. The high performance buffering technique of claim 15, wherein said initialization step comprises the step of:

writing the data into a location of said buffer as designated by a write pointer.

17. The high performance buffering technique of claim 15, wherein said transmit buffering step comprises the steps of:

incrementing a write pointer to prevent a next byte to be transmitted from overwriting a previous written byte; and

incrementing a write shift counter to facilitate tracking of a number of bytes available for transmission.

18. The high performance buffering technique of claim 15, wherein said transmit and receive shifting step comprises the steps of:

reading the data from a location in the buffer designated by a shift pointer;

writing the data to a transmit shift register;

shifting of the transmit shift register; and

receiving and storing the new data in a receive shift register in a location of said buffer designated by a read pointer.

19. The high performance buffering technique of claim 15, wherein said receive buffering step comprises the steps of:

incrementing a shift pointer to identify a new location in the buffer for receiving data; and

incrementing a read shift counter to indicate that the new data has been received.

20. The high performance buffering technique of claim 15, wherein said buffering technique further comprises the steps of:

interrupting a CPU if the data is ready for transmitting and said buffer is approximately full; and

interrupting the CPU if said buffer is ready to receive data and said buffer is approximately empty.

21. A high performance buffering technique for use with a serial peripheral interface to facilitate high data rates, said buffering technique comprising the steps of:

indicating a location in a single buffer where a CPU can write data to be transmitted;

indicating a location in said single buffer where any received data can be stored for reading by the CPU;

indicating a location where data to be transmitted is located and a location where the received data will be stored after shifting of any registers is completed;

tracking a number of bytes of data that need to be transmitted; and

tracking a number of bytes of data that have been received.